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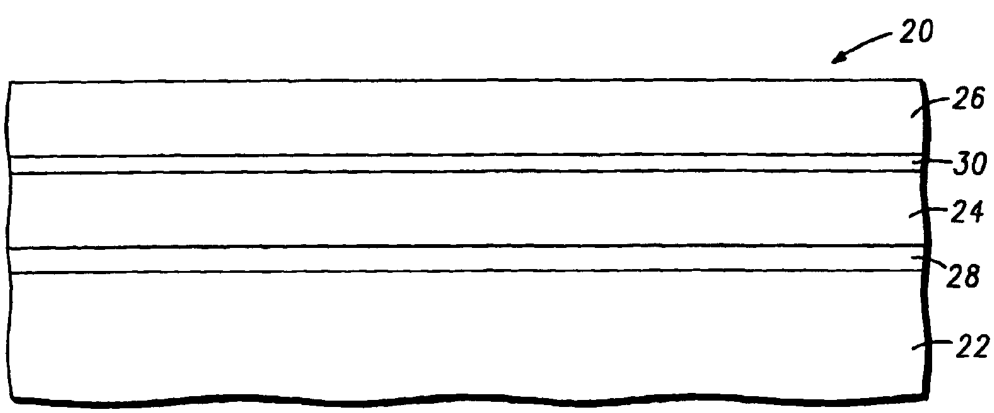
(54) Title: SEMICONDUCTOR STRUCTURE INCLUDING A MAGNETIC TUNNEL JUNCTION



(57) Abstract: High quality epitaxial layers of ferromagnetic materials can be grown overlying large silicon wafers (22) by first growing an accommodating buffer layer (24) on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer (28) of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer. This technique permits the fabrication of devices (96) employing ferromagnetic materials on a monocrystalline semiconductor substrate. In particular, magnetic tunnel junction devices may be fabricated on silicon in accordance with this technique.

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SEMICONDUCTOR STRUCTURE INCLUDING A MAGNETIC TUNNEL JUNCTION

Field of the Invention

The present invention relates generally to compound semiconductor structures and devices and to a method for their fabrication, and more specifically to magnetic tunnel junction (MTJ) structures and devices and to the fabrication of MTJ devices on a monocrystalline semiconductor substrate.

Background of the Invention

Magnetic tunnel junction (MTJ) devices have several applications in the microelectronics industry. For example, MTJ devices can be used to form magnetic non-volatile memory elements, magnetic field sensors, and the like.

MTJ devices generally include two ferromagnetic layers separated by a thin insulating layer. The MTJ devices are often fabricated by forming the ferromagnetic and insulating layers over strontium titanate substrates. Such substrates are relatively expensive and are generally available only in relatively small forms (*e.g.*, substrates having a diameter less than about two inches).

The performance of MTJ devices typically increases as the crystallinity of the ferromagnetic film increases. For example, an amount of change of resistance per amount of magnetic field applied to a ferromagnetic layer for a monocrystalline ferromagnetic material is typically higher than that of the same material in polycrystalline or amorphous form. In addition, sharp interfaces between the insulating and ferromagnetic layers tend to improve

performance of the MTJ device by reducing the noise of the device. Accordingly, methods for forming monocrystalline ferromagnetic and insulating materials, having sharp interfaces, on a substrate are desirable.

If a large area thin film of high quality monocrystalline ferromagnetic material was available at low cost, a variety of semiconductor devices could advantageously be fabricated using that film at a low cost compared to the higher cost of fabricating such devices on strontium titanate substrates. In addition, if a thin film of high quality monocrystalline ferromagnetic material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure could be achieved that took advantage of the best properties of both the silicon and the ferromagnetic material.

Accordingly, a need exists for a microelectronic structure that provides a high quality monocrystalline ferromagnetic film over another monocrystalline material such as a semiconductor wafer and for a process for making such a structure. In particular, a need exists for an MTJ device which can be grown epitaxially on a silicon substrate, thus reducing the cost of the MTJ devices and facilitating monolithic integration with the underlying silicon devices and circuits.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 - 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates schematically, in cross-section, a magnetic tunnel junction fabricated on a monocrystalline semiconductor substrate;

FIG 6 illustrates schematically, in cross-section, a magnetic tunnel junction stack fabricated on a monocrystalline semiconductor substrate;

FIG. 7 illustrates schematically, in cross-section, the device of FIG. 6 illustrating a template layer;

FIG. 8 illustrates schematically, in cross-section, the device of FIG. 6 illustrating monolithic integration between the magnetic tunnel junction and an integrated logic element formed in the monocrystalline semiconductor substrate; and

FIGS. 9-18 illustrate schematically, in cross-section, additional device structures in accordance with various embodiments of the invention.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a microelectronic structure 20 in accordance with an embodiment of the invention. Microelectronic structure 20 includes a monocrystalline substrate 22, an accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of ferromagnetic material, which is preferably monocrystalline. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and ferromagnetic material layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the ferromagnetic material layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and, by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and

preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Substrate 22 can also be of a compound semiconductor material. The compound semiconductor material of substrate 22 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like.

Preferably, substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate

layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in ferromagnetic material layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying metallic oxide material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and to the subsequently applied ferromagnetic material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements and have a perovskite crystal lattice structure. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22,

and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The ferromagnetic material of layer 26 can be selected, as desired for a particular structure or application. Exemplary materials suitable for ferromagnetic material layer 26 include a general chemical formula of $(A_xB_{1-x})CO_3$ where x ranges from 0 to 1 and where A is lanthanum or neodymium, B is strontium, barium, calcium, or lead, and C is Mn, (Mn_yCo_{1-y}) or (Mn_zNi_{1-z}) where y and z are greater than zero and less than one.

Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent ferromagnetic material layer 26. When used, template layer 30 has a thickness ranging from about one to about ten monolayers.

FIG. 2 illustrates, in cross section, a portion of a microelectronic structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described structure 20, except that an additional insulating layer 32 is positioned above ferromagnetic material 26 and a second additional layer of ferromagnetic material 33 is formed over insulating layer 32. Insulating material suitable for layer 32 may include any insulating material listed above in connection with accommodating buffer layer 24, and ferromagnetic material layer 33 may include any ferromagnetic material listed above in connection with layer 26. Layer 33 is typically about 1-6 nm and preferably less than about 2.5 nm.

FIG. 3 schematically illustrates, in cross section, a portion of a microelectronic structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 40, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and additional buffer layer 32 (subsequent to layer 32 formation) relieves stresses between layers 22 and 32 and provides a true compliant substrate for subsequent processing--*e.g.*, ferromagnetic material layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline ferromagnetic material layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline ferromagnetic material layers because it allows any strain in layer 32 to relax prior to forming layer 26.

In accordance with one embodiment of the present invention, layer 30 serves as an anneal cap during layer

36 formation and as a template for subsequent ferromagnetic material layer 26 formation. Accordingly, layer 30 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 30 to form as a substantially defect free monocrystalline layer (often less than about ten monolayers).

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, illustrated in FIG. 1, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_gBa_{1-g}TiO_3$ and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The composition of layer 24 is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nm and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the ferromagnetic layer from the substrate to obtain the desired properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, ferromagnetic material layer 26 is a layer of $LaSrMnO_3$ having a thickness of about 5 nm to about 500 and preferably a thickness of about 20 nm to about 70 nm. The thickness generally depends on the application for which the layer is being prepared.

Example 2

In accordance with another embodiment of the invention, illustrated in FIG. 3, a structure is provided that is suitable for MTJ applications. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_gBa_{1-g}TiO_3$, where g ranges from zero to one, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The ferromagnetic material can be, for example $LaSrMnO_3$, and layers 26 and 33 thickness can be about 5 nm to about 500 and preferably about 20 nm to about 70 nm. Layer 32, which is interposed between ferromagnetic layers 26 and 33 includes $Sr_gBa_{1-g}TiO_3$, where g ranges from zero to one, having a thickness of about 2.5 nm.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon or gallium arsenide substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the

growth of a high quality crystalline layer on the underlying layer.

FIG. 4 graphically illustrates the relationship of the achievable thickness of a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that has a large number of defects. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of

the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layers 26 and 33 are layers of epitaxially grown ferromagnetic material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials, this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. In some instances, a crystalline buffer layer between the host oxide and the grown metallic oxide layer can be used to reduce strain in the grown monocrystalline ferromagnetic material layer that might result from small differences in lattice constants. Better crystalline quality in the grown monocrystalline ferromagnetic material layer can thereby be achieved.

Insulating layer 32 is also characterized by a crystal lattice constant and a crystal orientation. In accordance with an embodiment of the invention, insulating material 32 is selected such that it can be orientates such that a lattice constant of layer 32 substantially matches the lattice constants for layers 26 and 33.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a microelectronic structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a

temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature, a solid state reaction takes place between the strontium oxide and the native silicon oxide, causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and

titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate may be capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired material. For example, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of the template (if one is formed), the ferromagnetic material is grown using MBE or other suitable techniques.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an

insulating layer deposition step. Insulating material for layer 32 may be epitaxially formed over layer 26 using the method described above in connection with layer 24 formation, with the exception that an amorphous interface layer is preferably not formed between layer 26 and layer 32. Accordingly, the insulating layer is preferably formed using condition that favor stochiometric growth of layer 26.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22 as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 32. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and layer 30 or a suitable cap layer to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36.

Ferromagnetic layer 52, *e.g.*, $(La_kSr_{1-k})MnO_3$, where k is greater than zero and less than one, is epitaxially grown using sputter deposition. More particularly, the $(La_kSr_{1-k})MnO_3$ layer is grown by RF magnetron sputtering (face to face configuration) from a $(La_kSr_{1-k})MnO_3$ target. The deposition is performed with oxygen as sputter gas, and a substrate temperature of about 400 °C.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a ferromagnetic material layer by the processes of molecular beam epitaxy and RF sputtering. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other metallic oxide layers can be deposited overlying the monocrystalline oxide accommodating buffer layer and/or the ferromagnetic layer.

Each of the variations of ferromagnetic material and monocrystalline oxide layers may use an appropriate template for initiating the growth of the respective layer. In such a case, suitable template materials may be grown according to the methods described above in connection with growing layer 26.

FIG. 5 illustrates schematically, in cross-section, a semiconductor structure 90 in accordance with the present invention. Semiconductor structure 90 includes a monocrystalline semiconductor substrate 92, a monocrystalline insulator layer 94 overlying substrate 92, and a magnetic tunnel junction device 96 overlying the insulator layer. In accordance with one embodiment of the present invention, insulator layer 94 is a monocrystalline oxide layer epitaxially grown over the substrate.

FIG. 6 illustrates schematically, in cross-section, a semiconductor structure 98 generally analogous to the structure shown in FIG. 5. In FIG. 6, a magnetic tunnel junction 96 is illustrated as a first layer 100 overlying insulator layer 94, a second layer 102 overlying first layer 100, and a third layer 104 overlying second layer 102. In accordance with one aspect of the present invention, first layer 100 and third layer 104 are capable of exhibiting ferromagnetic properties. In the illustrated embodiment, first layer 100 and second layer 102 may be epitaxially grown on their respective underlying layers. In addition, second layer 102 is advantageously a monocrystalline insulator layer. Moreover, one or both of first layer 100 and third layer 104 may also be monocrystalline layers. In a particularly preferred embodiment, substrate 92 is silicon. Insulator layer 94 is preferably a monocrystalline material selected from the group consisting of metal oxides and metal nitrides. More particularly, insulating layer 94 is preferably selected from the following materials: alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, gallium nitride, and aluminum nitride.

In a particularly preferred embodiment, first layer 100 is preferably a monocrystalline oxide, for example, a manganite perovskite, but may be made from any suitable material having a composition $(A,B)CO_3$ where A is selected form the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead, and C is selected from the group consisting of Mn, (Mn,Co), and (Mn,Ni).

Third layer 104 is preferably a monocrystalline oxide, for example, a manganite perovskite, but may also be made from any of the materials described above in connection with first layer 100. Second insulator layer 102 is preferably a monocrystalline oxide having a thickness in the range of 1 to 6 nm, and is preferably lattice matched to first layer 100. In a particularly preferred embodiment, second insulator layer 102 is at a thickness less than about 2.5 nm and is lattice matched within about four percent to first layer 100. In addition, second insulator layer 102 is preferably configured to provide an atomically sharp interface with first layer 100. Second insulator layer 102 may be made from a material selected from the group consisting of alkali earth metal titanites, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

In accordance with a further aspect of the present invention, first layer 100, second layer 102, and third layer 104 may be patterned to form, at least in part, a magnetic tunnel junction device in accordance with generally known fabrication techniques. By fabricating a magnetic tunnel junction device on a monocrystalline (*e.g.*, silicon) substrate 92 in accordance with the present invention, substantially reduced cost may be

realized by the scalability afforded by monocrystalline substrate 92.

FIG. 7 illustrates schematically, in cross-section, a semiconductor structure 106 similar to structure 98 shown in FIG. 6, but also including a template 118 overlying insulator layer 94. Template layer 118 advantageously terminates insulator layer 94 and may be made from oxygen and an element selected from strontium, barium, calcium, or lead. Template layer 118 is preferably in the range of 1 to 10 monolayers in thickness.

FIG. 8 illustrates schematically, in cross-section, a semiconductor structure 110 generally analogous to the structures shown in FIGS. 5 - 7, and further illustrating an integrated logic element 130, such as a metal oxide semiconductor (*e.g.*, CMOS) circuit formed at least partially in substrate 92. In a preferred embodiment, logic element 130 may be electrically connected to the magnetic tunnel junction by an interconnection 108. In the illustrated embodiment, interconnection 108 connects logic element 130 to second layer 102.

FIG. 9 illustrates schematically, in cross-section, a semiconductor structure 112 generally analogous to that shown in FIGS. 5 - 8. Semiconductor 112 includes a strain relief layer 114, for example, an amorphous oxide layer underlying insulator layer 94. In this regard, amorphous oxide layer 114 is generally analogous to intermediate layer 28 discussed above in connection with FIGS. 1 and 2.

FIG. 10 illustrates schematically, in cross-section, a semiconductor structure 116 generally analogous to structure 98 of FIG. 6. Semiconductor structure 116 includes magnetic tunnel junction 96 sandwiched between a first electrical contact layer 120 formed underlying and electrically contacting first layer 100, and a second electrical contact layer 122 overlying and electrically

contacting third layer 104. One or both of layers 120 and 122 preferably comprise a monocrystalline electrically conductive oxide layer, and be made from a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$, $SrRuO_3$, $SrCrO_3$, and $SrVO_3$, where k is greater than zero and less than one.

FIG. 11 illustrates schematically, in cross-section, a semiconductor structure 124 including a monocrystalline semiconductor (*e.g.*, silicon) substrate 92, a monocrystalline oxide layer 94, preferably epitaxially grown overlying substrate 92, and a magnetic tunnel junction device 96. Magnetic tunnel junction device 96 preferably includes a first layer 100 made of a monocrystalline ferromagnetic material, a second layer 102 made from a monocrystalline insulator material which overlies and forms an atomically sharp interface with first layer 100, and a third layer 104 made from a ferromagnetic material. Second layer 102 is preferably sufficiently thin to allow carrier tunneling therethru. Third layer 104 advantageously exhibits an ordered crystalline structure. In a preferred embodiment, first layer 100, second layer 102, and third layer 104 are each monocrystalline materials epitaxially grown on their underlying layer. Second layer 102 is preferably an electrically insulating oxide selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

FIG. 12, illustrates schematically, in cross-section, a semiconductor structure 126 including substrate 92 having logical element 130 formed at least partially therein, insulating layer 94 and magnetic tunnel junction 96. Semiconductor structure 126 further includes

amorphous oxide layer 114, and an electrical interconnect 132 configured to electrically couple logic element 130 to layer 104. Insulator layer 94 is preferably a monocrystalline oxide layer made from $Sr_gBa_{1-g}TiO_3$, where g ranges from zero to one. Monocrystalline layer 102 is preferably an oxide having a thickness in the range of 1 to 6 nm, and is advantageously lattice matched to within four percent of layer 100. The various semiconductor structure illustrated and described herein may be fabricated using any of the processing techniques described above in connection with FIGS. 1-3. By fabricating the magnetic tunnel junction devices discussed herein on monocrystalline semiconductor substrate 92, monolithic integration between the magnetic tunnel junction structure and microelectronic structures associated with substrate 92 is enabled.

FIG. 13, illustrates schematically, in cross-section, an integrated magnetic tunnel junction circuit 140. Semiconductor structure 140 includes a template layer 142 overlying substrate 92, as well as insulator layer 94. As described above in connection with FIGS. 1-3, amorphous oxide layer 114 is advantageously fabricated during the step of epitaxially growing insulator layer 94 on substrate 92. Thereafter, a second template layer 144 may be advantageously fabricated on insulator layer 94. Second template layer 144 facilitates the epitaxial growth of first ferromagnetic oxide layer 100. In accordance with the preferred embodiment, second insulative oxide layer 102 is preferably epitaxially grown on first ferromagnetic oxide layer 100.

Semiconductor structure 140 of FIG. 13 illustrates the photolithographic patterning of first layer 100, second layer 102 and third layer 104 to permit the magnetic tunnel junction to be monolithically integrated

with logic element 130 associated with substrate 92. In particular, an electrical interconnect 134 provides electrical contact between logic element 130 and each of first layer 100 and third layer 104. Specifically, interconnect 134 is configured to contact an electrode 136 associated with third layer 104 and an electrode 138 associated with first layer 100. In the context of illustrated embodiments, the monocrystalline layers may be grown using any suitable process, including MBE, MOCVD, MEE, CVD, PVD, PLD, CSD, and ALE. Indeed, these techniques may be employed to grow any of the layers illustrated herein, as appropriate.

In accordance with a further aspect of the present invention, a template layer may be formed by terminating the growth of the underlying monocrystalline layer with 1 to 10 monolayers of oxygen and a material selected from the group consisting of strontium, barium, calcium and lead.

A preferred method of fabricating a magnetic tunnel junction structure 146 will now be described in conjunction with FIG. 14. The monocrystalline silicon substrate 92 is first provided. Thereafter, a number of layers are sequentially deposited to form a semiconductor stack, using any combination of the deposition processes described herein. In a preferred embodiment, insulator layer 94 comprising a layer of $Sr_gBa_{1-g}TiO_3$, where g ranges from zero to one is deposited on substrate 92. Ferromagnetic layer 100 is then deposited on insulator layer 94, ferromagnetic layer 100 is preferably a material of the composition $(A,B)CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium and lead, and C is selected from the group consisting of Mn, (Mn,Co), and (Mn, Ni). Insulative tunnel oxide layer

102 is then deposited on layer 100. Ferromagnetic layer 104, suitably of a material similar to that of layer 100, is then deposited on layer 102.

FIG. 15, illustrates schematically, in cross-section, a semiconductor structure 156 generally analogous to structure 146 of FIG. 14 further illustrating amorphous layer 114 and logic element 130 formed at least partially within substrate 92.

FIG. 16 illustrates schematically, in cross-section, a semiconductor structure 158 generally analogous to structure 146 of FIG. 14 further illustrating the step of patterning one or more of layers 100, 102, and 104 to thereby yield respective nodes 150, 152 and 154, which may correspond to any desired combination of voltage or current nodes. Those skilled in the art will appreciate that patterning one or more of layers 100, 102 and 104 may produce a magnetic tunnel junction device of any desired configuration.

FIG. 17, illustrates schematically, in cross-section, a semiconductor structure 160 generally analogous to structure 158 of FIG. 16, further including the additional step of depositing a layer of conductive material 180 and patterning layer 180 to produce respective nodes 164, 166 and 168. In a particularly preferred embodiment, an interconnect 170 is suitably fabricated into semiconductor structure 160 to connect one or more of nodes (*e.g.*, electrodes) 164-168 with logic element 130. The processes and structures shown in FIGS. 12-17 illustrate, *inter alia*, the advantages of fabricating magnetic tunnel junction devices on a monocrystalline semiconductor substrate to thereby enable the monolithic integration of magnetic tunnel junction devices with logic elements associated with the substrate.

FIG. 18, illustrates schematically, in cross-section, a semiconductor structure 162 which includes the additional step of depositing a conductive oxide layer 172 over insulator 94 and an electrical contact with ferromagnetic layer 100. Conductive oxide layer 172 is preferably fabricated by the step of depositing a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$, $SrRuO_3$, $SrCrO_3$, and $SrVO_3$, where k is greater than zero and less than one.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

We claim:

1. A magnetic tunnel junction structure comprising:

a monocrystalline semiconductor substrate;

a monocrystalline insulator layer overlying the substrate;

a first layer epitaxially grown overlying the monocrystalline insulator layer, the first layer capable of exhibiting ferromagnetic properties;

a second monocrystalline insulator layer epitaxially grown overlying the first layer; and

a third layer overlying the second monocrystalline insulator layer, the third layer capable of exhibiting ferromagnetic properties.

2. The structure of claim 1 wherein the first layer is monocrystalline.

3. The structure of claim 2 wherein the third layer is monocrystalline.

4. The structure of claim 1 wherein the substrate comprises silicon.

5. The structure of claim 4 further comprising a CMOS circuit formed at least partially in the substrate.

6. The structure of claim 1 wherein the monocrystalline insulating layer comprises a material selected from the group consisting of metal oxides and metal nitrides.

7. The structure of claim 6 wherein the monocrystalline insulating layer comprises a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, gallium nitride, and aluminum nitride.

8. The structure of claim 6 wherein the first layer comprises a manganite perovskite.

9. The structure of claim 6 wherein the first layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

10. The structure of claim 9 wherein the first layer comprises a monocrystalline oxide.

11. The structure of claim 9 further comprising a template layer overlying the monocrystalline insulator layer.

12. The structure of claim 11 wherein the template layer terminates the monocrystalline insulator layer and comprises a layer comprising oxygen and an element selected from the group consisting of strontium, barium, calcium, and lead.

13. The structure of claim 12 wherein the template layer has a thickness of 1 - 10 monolayers.

14. The structure of claim 6 wherein the third layer comprises a manganite perovskite.

15. The structure of claim 6 wherein the third layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

16. The structure of claim 15 wherein the third layer comprises a monocrystalline oxide.

17. The structure of claim 6 wherein the second monocrystalline insulator layer comprises an oxide having a thickness of 1 - 6nm.

18. The structure of claim 17 wherein the second monocrystalline insulator layer comprises a material lattice matched to the first layer.

19. The structure of claim 6 wherein the second monocrystalline insulator layer comprises a monocrystalline oxide having a thickness less than 2.5nm and the oxide comprises a material lattice matched within about 4 percent to the first layer.

20. The structure of claim 1 wherein the second monocrystalline insulator layer is configured to provide an atomically sharp interface with the first layer.

21. The structure of claim 6 wherein the second monocrystalline insulator layer comprises a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

22. The structure of claim 21 wherein the second monocrystalline insulator layer comprises an alkali earth metal titanate.

23. The structure of claim 1 wherein the first layer, second monocrystalline insulator layer, and the third layer are patterned to form, in part, a magnetic tunnel junction device.

24. The structure of claim 23 further comprising an integrated logic element formed at least partially in the semiconductor substrate.

25. The structure of claim 24 further comprising an interconnection formed between and electrically interconnecting the integrated logic element and the magnetic tunnel junction device.

26. The structure of claim 1 further comprising an amorphous oxide strain relief layer formed underlying the monocrystalline insulator layer.

27. The structure of claim 1 further comprising a first electrical contact layer formed underlying and electrically contacting the first layer and a second electrical contact layer overlying and electrically contacting the third layer.

28. The structure of claim 27 wherein the first electrical contact layer comprises a monocrystalline electrically conductive oxide layer.

29. The structure of claim 28 wherein the first electrical contact layer comprises a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$ where k is greater than 0 and less than 1, $SrRuO_3$, $SrCrO_3$, and $SrVO_3$.

30. A magnetic tunnel junction structure comprising:

a monocrystalline semiconductor substrate;

a monocrystalline oxide layer epitaxially grown overlying the substrate;

a first layer of monocrystalline ferromagnetic material overlying the monocrystalline oxide layer;

a second layer of monocrystalline insulator material overlying the first layer and forming an atomically sharp interface with the first layer, the second layer sufficiently thin to allow carrier tunneling therethrough; and

a third layer of ferromagnetic material overlying the second layer.

31. The structure of claim 30 wherein the third layer comprises a layer of material having an ordered crystalline structure.

32. The structure of claim 30 wherein each of the first layer, second layer, and third layer comprises a layer of epitaxially grown monocrystalline material.

33. The structure of claim 30 wherein the first layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

34. The structure of claim 33 wherein the second layer comprises an electrically insulating oxide selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

35. The structure of claim 34 wherein the third layer comprises a material having a composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

36. An integrated magnetic tunnel junction circuit comprising:

a monocrystalline silicon substrate;

an integrated logic circuit formed at least partially in the silicon substrate;

a first monocrystalline oxide layer epitaxially grown overlying the silicon substrate;

an amorphous oxide formed underlying the first monocrystalline oxide layer;

a second monocrystalline oxide layer comprising a ferromagnetic material epitaxially formed overlying the first monocrystalline oxide layer;

a third monocrystalline oxide layer comprising an electrically insulative material overlying the second monocrystalline oxide layer, the third monocrystalline oxide layer sufficiently thin to allow carrier tunneling therethrough;

a fourth layer of oxide comprising a ferromagnetic material formed overlying the third monocrystalline oxide layer; and

an electrical interconnect coupling the integrated logic circuit and the fourth monocrystalline oxide layer.

37. The circuit of claim 36 wherein the integrated logic circuit comprises a CMOS circuit.

38. The circuit of claim 36 wherein the first monocrystalline oxide layer comprises a material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

39. The circuit of claim 38 wherein the first monocrystalline oxide layer comprises an alkali earth metal titanate.

40. The circuit of claim 38 wherein the first monocrystalline oxide layer comprises $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1.

41. The circuit of claim 38 wherein the second monocrystalline oxide layer comprises $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

42. The circuit of claim 41 wherein the fourth oxide layer comprises $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

43. The circuit of claim 38 wherein the third monocrystalline oxide layer comprises an insulative oxide material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, perovskites including tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

44. The circuit of claim 43 wherein the third monocrystalline oxide layer comprises an oxide having a thickness between 1nm and 6nm.

45. The circuit of claim 43 wherein the third monocrystalline oxide layer comprises an oxide lattice matched to within 4 percent to the second monocrystalline oxide layer.

46. A process for fabricating an integrated magnetic tunnel junction circuit comprising the steps of:

providing a monocrystalline semiconductor substrate;

forming an integrated logic circuit at least partially in the semiconductor substrate;

forming a first template layer overlying the semiconductor substrate;

epitaxially growing a monocrystalline insulator layer overlying the first template layer;

forming an amorphous oxide layer underlying the monocrystalline insulator layer during the step of epitaxially growing the monocrystalline insulator layer;

forming a second template layer overlying the monocrystalline insulator layer;

epitaxially growing a first ferromagnetic oxide layer overlying the second template layer;

epitaxially growing a second monocrystalline insulative oxide layer overlying the first ferromagnetic oxide layer;

growing a second ferromagnetic oxide layer overlying the electrically conductive oxide layer;

photolithographically patterning the first ferromagnetic oxide layer, the second monocrystalline

insulative oxide layer and the second ferromagnetic oxide layer to expose a portion of the integrated logic circuit;

forming electrodes contacting the first ferromagnetic oxide layer and the second ferromagnetic oxide layer; and

forming an electrical interconnect extending from the portion of the integrated logic circuit to the electrodes.

47. The process of claim 46 wherein the step of providing a monocrystalline semiconductor substrate comprises the step of providing a substrate comprising silicon having a silicon oxide layer on a surface thereof and the step of forming a first template layer comprises the steps of:

depositing a material from the group consisting of alkali earth metals and alkali earth metal oxides onto the silicon oxide layer and

heating the substrate to react the material with the silicon oxide.

48. The process of claim 47 wherein the step of depositing a material from the group consisting of alkali earth metals and alkali earth metal oxides comprises the step of depositing a material from the group consisting of barium, strontium, and mixtures of barium and strontium, and barium oxide, strontium oxide, and barium strontium oxide.

49. The process of claim 48 wherein the step of epitaxially growing a monocrystalline insulator layer comprises the steps of:

heating the monocrystalline semiconductor substrate to a temperature between about 200°C and about 800°C; and

introducing reactants comprising titanium, oxygen, and an element selected from strontium, barium, and strontium and barium.

50. The process of claim 49 wherein the step of introducing comprises controlling the ratio of strontium or barium to titanium and controlling the partial pressure of oxygen.

51. The process of claim 50 wherein the step of forming an amorphous oxide layer comprises increasing the partial pressure of oxygen above a level necessary for epitaxially growing the monocrystalline insulator layer.

52. The process of claim 49 wherein the step of forming a second template layer comprises the step of capping the monocrystalline oxide layer with a layer comprising a monolayer of a material selected from the group consisting of titanium, titanium and oxygen, strontium, strontium and oxygen, barium, and barium and oxygen.

53. The process of claim 46 wherein the step of growing a monocrystalline insulator layer comprises the step of epitaxially growing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

54. The process of claim 46 wherein the steps of epitaxially growing a first ferromagnetic oxide layer, epitaxially growing a second monocrystalline insulative oxide layer, and growing a second ferromagnetic oxide layer each comprise the step of epitaxially growing by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

55. The process of claim 46 wherein the step of epitaxially growing a first ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

56. The process of claim 46 wherein the step of growing a second ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

57. The process of claim 46 wherein the step of epitaxially growing a second monocrystalline insulative oxide layer comprises the step of growing a layer comprising an insulative material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

58. The process of claim 46 wherein the step of epitaxially growing a monocrystalline insulator layer comprises the step of growing a layer comprising an insulator material selected from the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates and vanadates, tin based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, gallium nitride, and aluminum nitride.

59. The process of claim 58 wherein the step of epitaxially growing a first ferromagnetic oxide layer comprises the step of growing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

60. The process of claim 59 wherein the step of forming a first template layer comprises the step of terminating the growth of the monocrystalline insulator layer with 1 - 10 monolayers of oxygen and a material selected from the group consisting of strontium, barium, calcium, and lead.

61. The process of claim 46 wherein the step of growing a second ferromagnetic material comprises the step of sputter depositing an oxide layer of composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

62. A process for fabricating a magnetic tunnel junction comprising the steps of:

providing a monocrystalline semiconductor substrate having a surface;

epitaxially growing a monocrystalline layer of insulator material on the surface;

epitaxially growing a first layer of ferromagnetic material overlying the monocrystalline layer of insulator material;

epitaxially growing a second layer of monocrystalline insulator oxide overlying the first layer; and

forming a second layer of ferromagnetic material overlying the second layer of monocrystalline insulator oxide.

63. The process of claim 62 wherein the step of epitaxially growing a first layer of ferromagnetic material comprises the step epitaxially growing a first layer of ferromagnetic material by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE.

64. The process of claim 63 wherein the step of epitaxially growing a first layer of ferromagnetic material comprises epitaxially growing a monocrystalline layer of ferromagnetic material.

65. The process of claim 62 wherein the step of forming a second layer of ferromagnetic material comprises the step of forming a second layer by PVD.

66. The process of claim 65 wherein the step of forming a second layer comprises the step of forming a layer having an ordered crystalline structure.

67. The process of claim 62 wherein the step of epitaxially growing a second layer of monocrystalline insulator oxide comprises the step of growing a layer of alkali earth metal oxide having a thickness of 1 - 6nm.

68. The process of claim 62 wherein the step of epitaxially growing a second layer of monocrystalline insulator oxide comprises the step of growing a layer of oxide sufficiently thin to allow carrier tunneling therethrough.

69. The process of claim 62 wherein the step of epitaxially growing a second layer of monocrystalline insulator oxide comprises the step of growing a layer of oxide lattice matched to within 4 percent to the first layer of ferromagnetic material.

70. The process of claim 69 wherein the step of epitaxially growing a second layer of monocrystalline insulator oxide comprises the step of growing a layer having a thickness less than 2.5nm.

71. A process for fabricating a magnetic tunnel junction circuit comprising the steps of:

providing a monocrystalline silicon substrate; and

depositing sequentially, by a process selected from the group consisting of MBE, MOCVD, MEE, CVD, PVD, PLD, CSD and ALE, the following monocrystalline epitaxial layers:

a layer of $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1;

a layer of ferromagnetic material of the composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1;

a layer of insulative tunnel oxide; and

a second layer of ferromagnetic material of the composition $(A_xB_{1-x})CO_3$ where A is selected from the group consisting of lanthanum and neodymium, B is selected from the group consisting of strontium, barium, calcium, and lead and x ranges from 0 to 1, and C is selected from the group consisting of Mn, (Mn_yCo_{1-y}) where y is greater than zero and less than or equal to 1, and (Mn_zNi_{1-z}) where z is greater than 0 and equal to or less than 1.

72. The process of claim 71 further comprising the step of forming a CMOS circuit at least partially in the silicon substrate.

73. The process of claim 71 further comprising the step of forming a strain relief layer underlying the layer of $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1.

74. The process of claim 71 further comprising the step of patterning the layer of ferromagnetic material, the layer of insulative tunnel oxide, and the second layer of ferromagnetic material to form a magnetic tunnel junction device.

75. The process of claim 74 further comprising the steps of:

depositing a layer of conductor material overlying the magnetic tunnel junction device and the CMOS circuit; and

patterning the layer of conductor material to form an electrical interconnect configured to electrically couple the CMOS circuit and the magnetic tunnel junction device.

76. The process of claim 71 wherein the step of depositing a layer of insulative tunnel oxide comprises the step of epitaxially growing a layer of monocrystalline alkali earth metal oxide having a thickness of 1 - 6nm.

77. The process of claim 71 wherein the step of depositing a layer of insulative tunnel oxide comprises the step of growing a layer of oxide sufficiently thin to allow carrier tunneling therethrough.

78. The process of claim 71 wherein the step of depositing a layer of insulative tunnel oxide comprises the step of growing a layer of oxide lattice matched to within 4 percent to the first layer of ferromagnetic material.

79. The process of claim 71 further comprising the step of epitaxially depositing a monocrystalline conductive oxide layer overlying the layer of $Sr_gBa_{1-g}TiO_3$ where g ranges from 0 to 1and electrically contacting the layer of ferromagnetic material.

80. The process of claim 79 wherein the step of epitaxially depositing a monocrystalline conductive oxide layer comprises the step of depositing a material selected from the group consisting of $(La_kSr_{1-k})CoO_3$ where k is greater than 0 and less than 1, $SrRuO_3$, $SrCrO_3$, and $SrVO_3$.

81. A magnetic tunnel junction structure comprising:

a monocrystalline silicon substrate;

a monocrystalline oxide layer epitaxially grown overlying the substrate; and

a magnetic tunnel junction device grown epitaxially overlying the monocrystalline oxide layer.

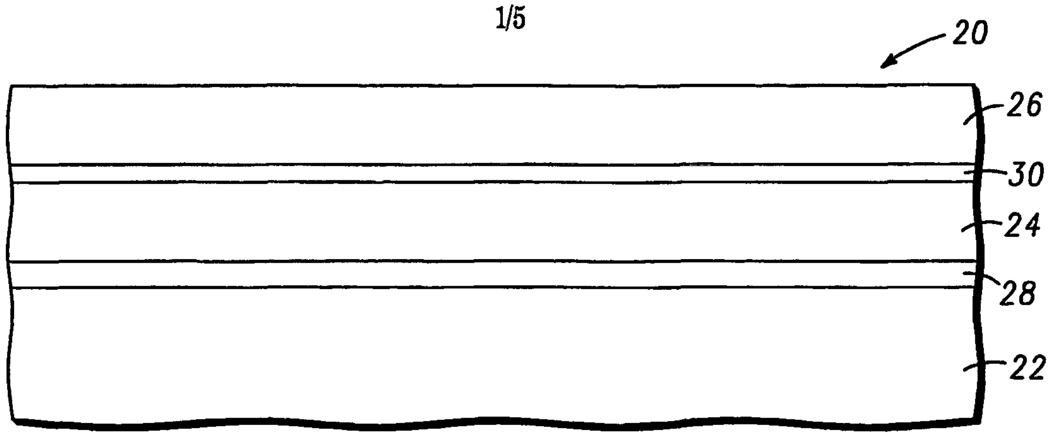

FIG. 1

FIG. 2

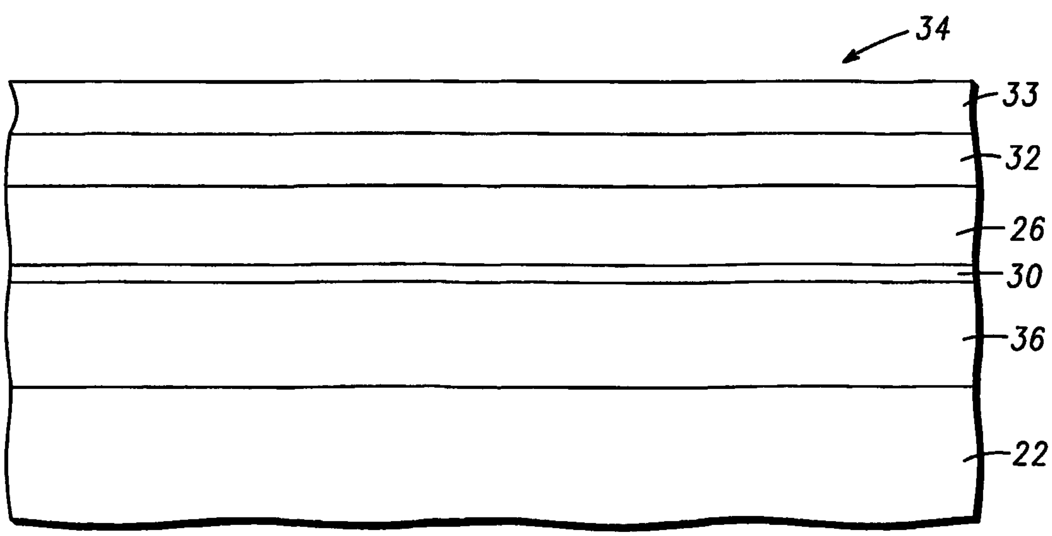

FIG. 3

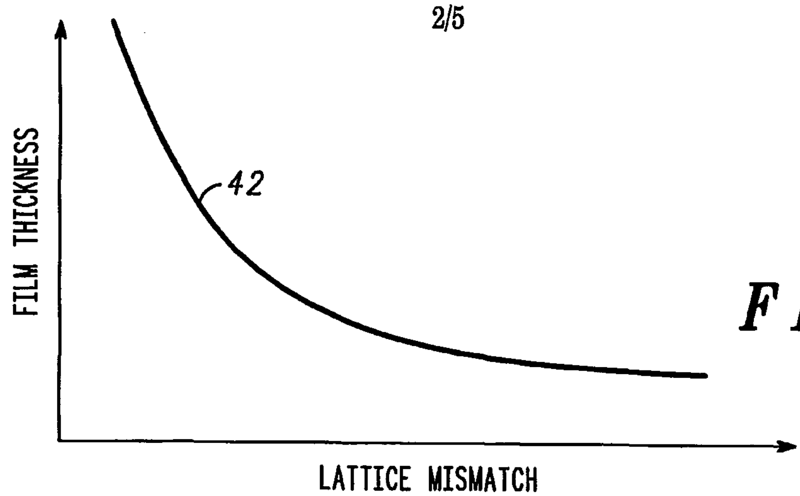

FIG. 4

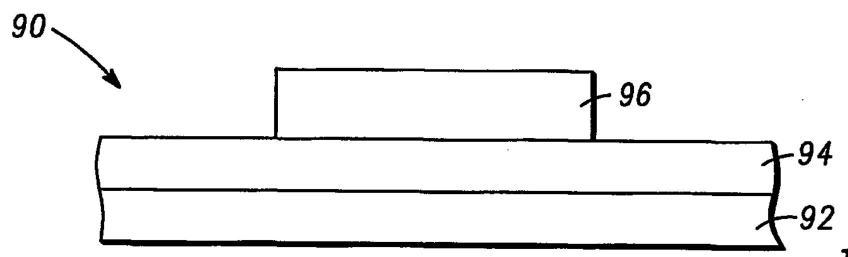

FIG. 5

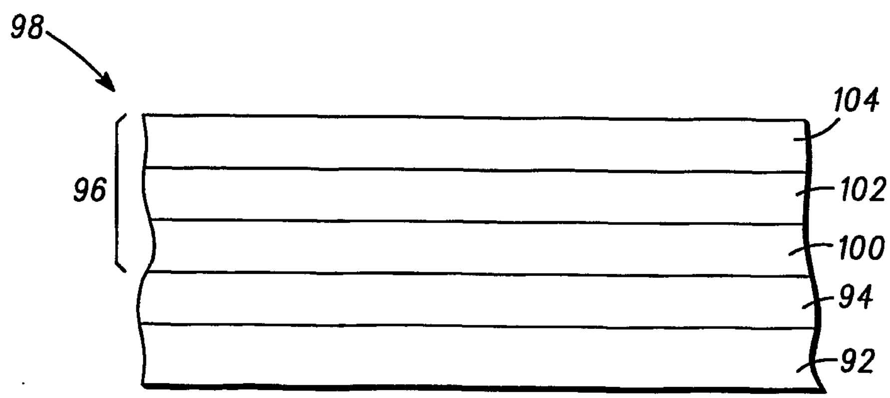

FIG. 6

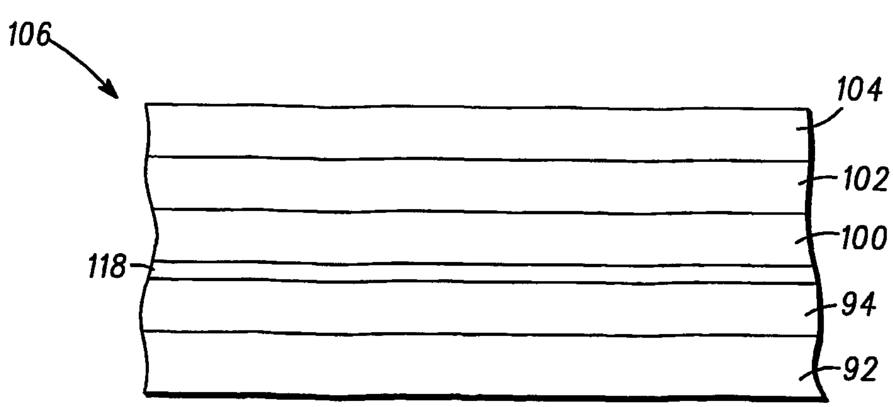

FIG. 7

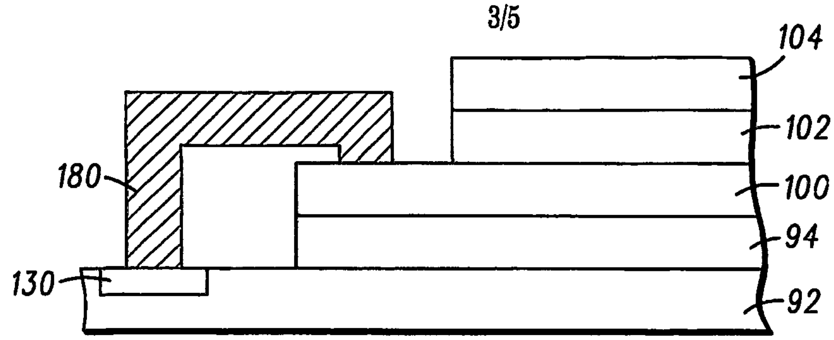

FIG. 8

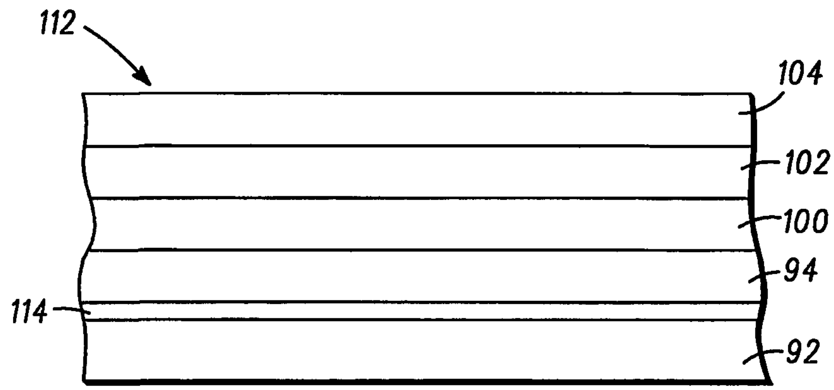

FIG. 9

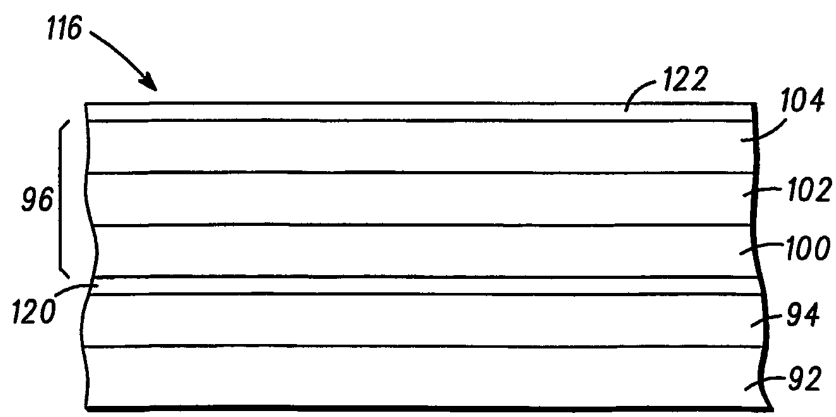

FIG. 10

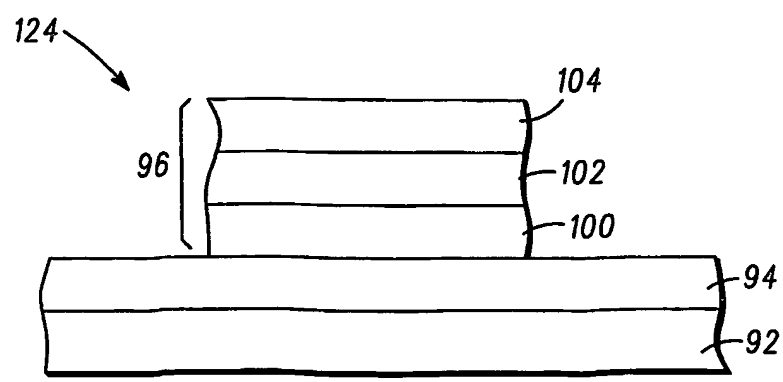

FIG. 11

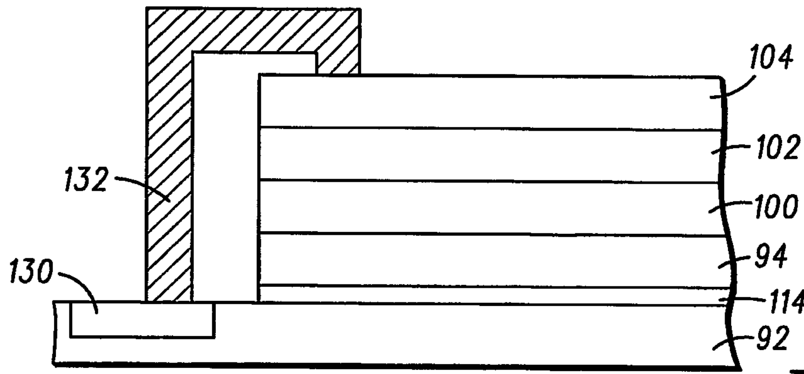

FIG. 12

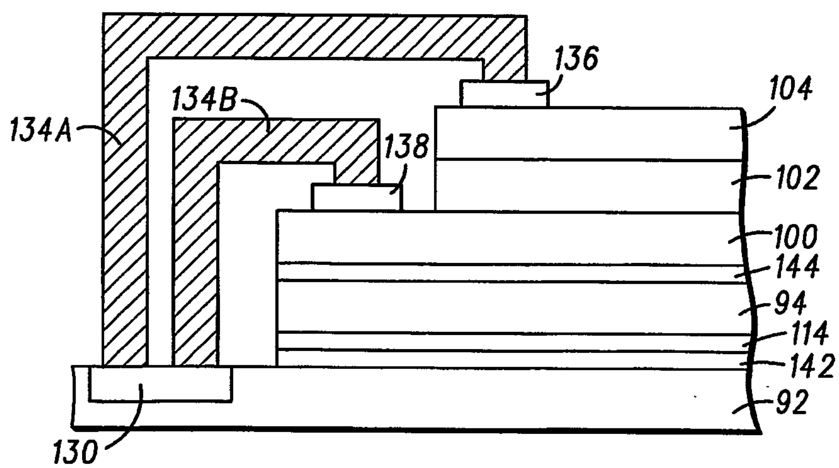

FIG. 13

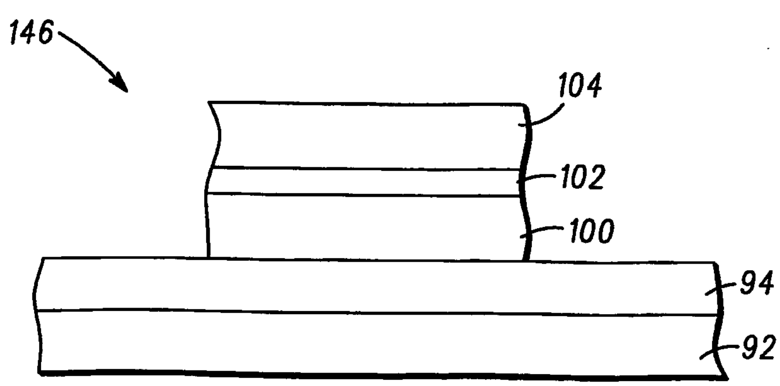

FIG. 14

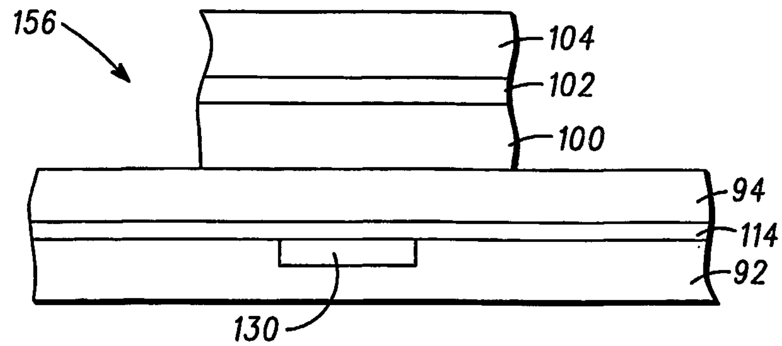

FIG. 15

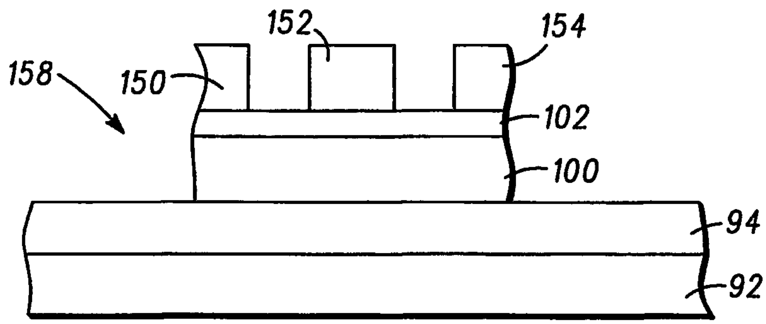

FIG. 16

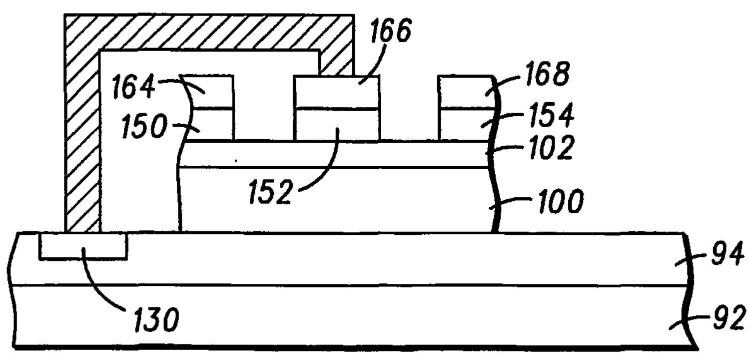

FIG. 17

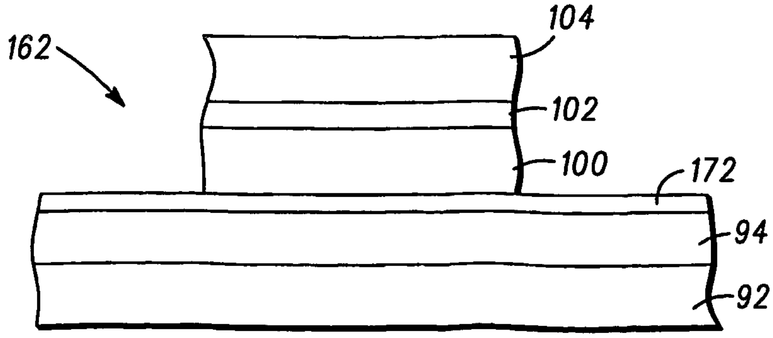

FIG. 18